THESIS DEFENCE

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Title: Creation of Electric Double Layer in Thin Film Transistors with charge carriers to achieve low voltage operation

Date: 10th, January, 2017

Time: 04:00 PM

Place: Samtel Centre Seminar Room (access from ground level)

Abstract: Thin film transistors (TFTs) are being developed for a wide range of innovative applications including active matrix LCD and OLED displays, RFIDs, sensor arrays due to the potential advantages of low cost fabrication using roll-to-roll printing techniques on flexible substrate. Among important characteristics of TFT, a sufficiently large channel current at low operating voltage is required to address many of the applications. As a result of low field effect mobility in amorphous semiconductors compounded with thick dielectric layers with low dielectric constant, a large operating voltage is normally needed to obtain adequate channel current. As a solution to this problem, in the present work, a new transistor design is proposed in which channel is created through formation of an Electric Double Layer (EDL) induced by electrons and holes. It is shown that when insulator is replaced by a semi-conducting layer of appropriate characteristics, large channel charge can be obtained at low operating voltage. Due to close proximity of mobile carriers, there is recombination and gate current which also determines the magnitude of channel charge. As a result, the proposed device is called a 'Current Induced Channel Transistor' (CICT) to contrast it with devices where channel is created through the field effect principle. The operation and limitations of the proposed transistor and performance of basic circuit blocks including display pixel circuits are illustrated through device-circuit mixed mode simulations. The thesis also presents an alternative realization of EDL based TFT structure in which high effective gate capacitance and associated large drain current at low operating voltage is achieved through creation of a trap assisted electric double layer at the interface. The use of dopants acting as traps ensures low recombination and high channel charge density.

Simulation results are presented that validate the proposed mechanism and indicate that current enhancement by a factor of almost an order can be achieved with a trap density of 1019cm-3 at 0.3eV above HOMO placed 5nm away from the semiconductor/dielectric interface. Experimental evidence for the proposed concept was observed in amorphous-IGZO TFT with e-beam evaporated SiO2 which exhibited an order of magnitude higher drain current than expected from typical values of mobility. Although the drain current enhancement was observed due to naturally present traps within an unoptimized dielectric, the results point to the feasibility of obtaining high output current through deliberate incorporation of traps in the dielectric leading to formation of a trap-assisted electric double layer.